

## **LISTING OF CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor member having thereon a plurality of electrode terminals; and

a mounting member having a plurality of interconnect pads electrically and mechanically connected to the respective electrode terminals for mounting the semiconductor member on the mounting member,

the interconnect pads forming a plurality of I/O cells including signal terminals, a portion of the I/O cells forming a first group of I/O cells and another portion of the I/O cells forming a second group of I/O cells disposed on an inner position of the mounting member with respect to the first group of I/O cells, the first group of I/O cells including a plurality of rows of interconnect pads disposed to encircle a center of the mounting member, and the second group of I/O cells including a plurality of rows of interconnect pads disposed to encircle a center of the mounting member, the first and second groups of I/O cells being disposed directly under the semiconductor member, wherein:

the first group of I/O cells are arranged in a first row and a second row disposed on an inner position relative to the first row,

the second group of I/O cells are arranged in a first row and a second row disposed on an inner position relative to the first row,

each of the first and second rows of the first group of I/O cells is arranged parallel to an outer periphery of the semiconductor member, and

each of the first and second rows of the second group of I/O cells is arranged parallel to the outer periphery of the semiconductor member.

2. (Original) The semiconductor device as defined in claim 1, wherein the semiconductor member is a semiconductor chip, the electrode terminals are internal electrodes disposed on a bottom surface of the semiconductor chip, and the mounting member is a package substrate used for packaging thereon the semiconductor chip.

3. (Previously Presented) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting the semiconductor member on a mounting substrate, the semiconductor package includes ball electrodes disposed on a bottom surface of a packaging substrate, and the mounting substrate forms a specified circuit by mounting the semiconductor package thereon.

4. (Previously Presented) The semiconductor device as defined in claim 1, wherein the I/O cells include only the signals terminals or terminals for signals, power and ground intermingled among one another.

5. (Previously Presented) The semiconductor device as defined in claim 4, wherein the I/O cells include peripherals.

6. (Previously Presented) The semiconductor device as defined in claim 1, wherein an interconnect line is electrically connected to each of the interconnect pads, and the interconnect lines electrically connected to the interconnect pads of at least one of the I/O cells are formed in a single interconnect layer.

7. (Previously Presented) The semiconductor device as defined in claim 6, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads in the single interconnect layer are formed on the surface of a packaging substrate.
8. (Previously Presented) The semiconductor device as defined in claim 7, wherein the interconnect lines connected to the I/O cells located on inner positions extend between the I/O cells located on an outer periphery.
9. (Original) The semiconductor device as defined in claim 6, wherein the interconnect pads and the interconnect lines electrically connected to the interconnect pads are formed as a multi-layered interconnect layer in the substrate.
10. (Original) The semiconductor device as defined in claim 9, wherein at least one of the first group and the second group includes an outer group and an inner group disposed on the inner position of the mounting member with respect to the outer group.
11. (Previously Presented) The semiconductor device as defined in claim 10, wherein the interconnect lines electrically connected to the interconnect pads corresponding to the first group of I/O cells and the interconnect lines electrically connected to the interconnect pads corresponding to the second group of I/O cells are formed in different interconnect layers.